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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/776,387	02/02/2001	Stanley N. Protigal	2898.2US (88-070.7)	2208

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/776,387	Applicant(s) PROTIGAL ET AL.	
	Examiner A. Sefer	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-6 and 8-10* is/are allowed.

6)☒ Claim(s) *1, 2 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on January 9, 2002 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of US Patent No. 6,184,568 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto (JP 61-73367).

Matsumoto discloses a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate 1; and a semiconductor device secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Onishi US Patent No. 4,477,736.

Onishi discloses in figs. 9 and 10 a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate 11; and a semiconductor device secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device.

5. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Muggli et al. US Patent No. 4,720,467.

Muggli et al disclose a semiconductor device system configured for electrical connection to external circuitry, the semiconductor device system comprising a carrier substrate 21; and a semiconductor device secured and operably coupled to the carrier substrate and including a semiconductor substrate having active circuit devices thereon; and an on-chip capacitor 20 including at least a portion thereof being formed in an active area of the semiconductor substrate, the on-chip capacitor being operably coupled between the active devices and the carrier substrate to provide filtering capacitance for the semiconductor device

6. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Matsumoto (JP 61-73367).

Matsumoto discloses a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate 1; active circuit devices on the semiconductor substrate; and a capacitor having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate.

7. Claim 2 is rejected under 35 U.S.C. 102(b) as being anticipated by Onishi US Patent No. 4,477,736.

Onishi discloses in figs. 9 and 10 a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate 11; active circuit devices on the semiconductor substrate; and a capacitor having at least a portion thereof formed in an active area of the

semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate.

8. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Muggli et al. US Patent No. 4,720,467.

Muggli et al disclose a semiconductor device for operable connection to a carrier substrate, the semiconductor device comprising, a semiconductor substrate 21; active circuit devices on the semiconductor substrate; and a capacitor 20 having at least a portion thereof formed in an active area of the semiconductor substrate, the capacitor being operably coupled to the active circuit devices to provide filtering capacitance when the semiconductor device is operably connected to a carrier substrate.

9. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Kachi (JP 58-77251).

Kachi discloses in fig. 2 a semiconductor device for connection to a carrier substrate configured power and ground thereto, the semiconductor device comprising a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor 4 on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefore when the semiconductor device is operably connected to a carrier substrate.

10. Claim 7 is rejected under 35 U.S.C. 102(b) as being anticipated by Onishi US Patent No. 4,477,736.

Onishi discloses in figs. 9 and 10 a semiconductor device for connection to a carrier substrate configured power and ground thereto, the semiconductor device comprising a semiconductor substrate having active circuit elements formed on an active areas thereof; at least one capacitor on the semiconductor substrate, at least a portion of the at least one capacitor being formed on the active area, the at least one capacitor operably connected to the active circuit elements to provide filtering capacitance therefore when the semiconductor device is operably connected to a carrier substrate.

Allowable Subject Matter

11. Claims 3-6 and 8-10 are allowed.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Shu et al US Patent No. 4,634,894 disclose a low power reference drivers formed on an IC chip.

b. IBM technical bulletin Vol. 30 No. 3 discloses an On-chip decoupling capacitor for VLSI chips.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
March 25, 2002